

Summary of Research Work

August 2010

The research contributions can be classified into two major areas: Nanoelectronics device technology and Integrated MEMS sensors. The research work includes materials and process technology development, device physics and modeling, circuits and system design.

Recently we have proposed sulphur passivation technique to de-pin the Fermi level for Schottky contacts on Germanium. This was a classic problem in Si/Ge semiconductor technology for the last six decades. We have experimentally demonstrated near-ideal Schottky barrier heights and achieved the highest electron barrier height, reported till date with Al-pGe. This has opened up the possibility of highly scaled Ge n-channel MOSFETs with Schottky source/drain junctions.

We have developed ultra thin (Effective Oxide Thickness < 1nm) rare earth metal oxide gate dielectrics (Gd_2O_3 , Er_2O_3) using RF sputtering and MOCVD, meeting the leakage current specifications for sub-45nm CMOS technologies.

New device structures, such as double gate transistors with ultra-thin body silicon channel, have been investigated with tight binding, ten orbital $sp^3d^5s^*$ band structure analysis. We have provided new insights into the “volume inversion” phenomenon and demonstrated that the double gate transistor can result in significantly higher performance. We have designed a novel Hybrid FinFET device with III-V channel material for sub 32nm technology nodes. The proposed device results in very high on current comparable to HEMT operation, simultaneously retaining the advantages of MOSFET in terms of very low leakage current. We have recently proposed, for the first time, a theoretical lower limit for the sub-threshold slope in Graphene transistors, based on self consistent solution of band structure and electrostatics, in double gate graphene transistor. We have also predicted the field induced band gap variations in Graphene nano ribbons, and demonstrated that the direct band gap transitions to indirect band gap under appropriate gating condition.

Transistor mismatch, or the inability to form tiny nano-transistors which are electrically alike, has become a major reliability problem for sub-100nm CMOS technology due to the statistical nature of semiconductor processes. The research work explores tackling this issue in the process technology realm as well as circuit design realm. Mixed mode simulation approach has been used to identify the relationship between process variable and circuit metric. Several statistical concepts such as design of experiments, response surface methodology and Monte-Carlo analysis are used to characterize a given process technology. Process Compact Models (PCM) have been derived which enable us to perform process sensitivity analysis and predict the delay distribution of a complex circuit such as a multiplier. We have proposed a novel speed and yield enhancement technique for semiconductor memories, which can correct the process variations post-facto. This has already resulted in an US patent. Recently we have proposed a novel “rate sensing keeper” technique applicable to all dynamic circuits, which are essential building blocks of high speed chips such as microprocessors. This idea has been successfully validated on 130nm Silicon CMOS technology and we have obtained an US patent on this aspect.

RF CMOS device modeling and circuit design is extremely important for communication applications. The non-quasi-static effect in CMOS transistors and its possible

effect on RF performance has been studied. The gate to source/drain overlap length has been optimized to yield an optimum unity gain transition frequency and noise figure. We have also developed a novel torsional MEMS varactor for RF applications, which provides the highest dynamic range reported till date.

The other major contribution in the area of sensors has been the design of very high performance sensor interface electronics circuits. The universal capacitance sensor chip, capable of measuring sub-femto Farad capacitance, has been prototyped on silicon. This has application for accelerometers, gyroscope and ultrasound transducers. We have developed a platform technology for gas sensors – consisting of micro-machined poly-silicon micro heater, RF sputtered SnO₂ thin film transducer, and ultra low power resistance read-out ASIC in 130nm CMOS technology with the realization of sub-threshold analog circuit. The circuit consumes 326 μ W power, which is the lowest reported till date for such applications. We have demonstrated this platform for LPG gas sensing. We have also achieved sub-10ppm ethanol sensing capability, using solution processed ZnO films.

We have recently proposed a very novel sensor architecture utilizing a suspended gate Silicon On Insulator (SOI) MOSFET operating in sub-threshold region. Since the transistor drain current is an exponential function of the gate voltage in this region of operation, the linear displacement in suspended gate results in an exponential response. This will potentially result in high resolution sensors for a variety of applications. Based on this concept, three international patent applications have been filed for gyroscope, microphone and gas sensor applications.