NANOELECTRONICS: AN OVERVIEW

Navakanta Bhat and Juzer Vasi

After completing his B.E. from the University of Mysore and M.Tech. from I.I.T. Bombay, Professor Bhat did his Ph. D. in Electrical Engineering from Stanford University in 1996. He then worked at Motorola’s Networking and Computing Systems Group in Austin, TX. He joined the Indian Institute of Science, Bangalore in 1999 where he is currently a Professor in the Centre for Nano Science and Engineering and Electrical Communication Engineering department. His current research is focused Nano-CMOS technology and Integrated CMOS-MEMS sensors. He has received the Young Engineer Award (2003) from INAE, Swarnajayanti fellowship (2005) from the DST and Prof. Satish Dhavan award (2005) from the Govt. of Karnataka. He is also the recipient of IBM Faculty award 2007. He is a Distinguished Lecturer of the IEEE Electron Devices Society. He is the Chairman of the Human Resource Development and Infrastructure committee of the National Program on Micro and Smart Systems.

Juzer Vasi obtained his B.Tech. in Electrical Engineering from the Indian Institute of Technology Bombay and the Ph.D. from The Johns Hopkins University. Since 1981, he has been at IIT Bombay, where he is currently the P. K. Kelkar Chair Professor of Nanotechnology. His research interests are in the area of semiconductor devices and technology, including nano-scale MOS devices, semiconductor-based non-volatile memories, and nanostructured photovoltaic devices. He was Editor of the IEEE Transactions on Electron Devices during 1997-2003, and a Distinguished Lecturer of the IEEE Electron Devices Society from 2001 to 2006. He is a Fellow of IEE, a Fellow of IETE, and a Fellow of the Indian National Academy of Engineering (INAE).

Introduction:
The phenomenal growth in the CMOS technology over the past four decades has enabled very high performance compute and storage systems, powering the information technology revolution. The MOS transistor has meta-morphed from dimensions of a few tens of microns in 1970s to a few tens of nanometers today. Semiconductor memory and high performance logic circuits have been the technology drivers to architect the miniaturization of the MOS transistor and this will continue in the foreseeable future. Today, we have 45 nm logic and memory technology in volume production enabling GHz microprocessors and Gbit memories. Moore’s law [Moore 1965, Bandyopadhyay 1998] has continued to work, albeit with several technological innovations. The underlying premise of this growth is the ability to scale down the MOS transistor dimension by 30%, in every two year cycle on an average. The Constant Electric Field scaling theory was proposed by Dennard in 1974 [Dennard 1974]. The scaling principle is to reduce the device operating voltage and all the linear dimensions of the device by a scaling factor, $k$ ($k > 1$), while simultaneously increasing the substrate doping concentration by the same scaling factor, $k$. The increase in the doping concentration is required to scale down the depletion width, an important linear dimension. This ensures that the electric field remains invariant in the scaled device. Fig.1 illustrates the scaling theory. The most important consequence of the
scaling is the impact on basic circuit parameters. The circuit delay \( \frac{=CV}{I} \) and power dissipation \( P=VI \) scale down by the factor \( k' \) respectively. The power delay product, which represents energy consumed per unit logic operation goes down as \( k'^2 \). Hence the circuits and systems built on scaled CMOS technology will be very efficient, besides resulting in very low form factor. The CMOS device scaling trend over the years is illustrated in Fig. 2. It is interesting to note that the linear dimensions of the device have scaled aggressively, however the supply voltage scaling \( V \) has been very slow due to the constraints imposed by system compatibility. This is often referred to as Generalized scaling as opposed to Constant Field scaling.

\[
P = V I \text{ } k \text{ } k
\]

For \( \Delta L=W \) condition, this can be simplified as

\[
V_{TH} = V_{THO} - \frac{Q_D}{C_\alpha} \frac{2}{L_G} \sqrt{\frac{\varepsilon_S \Phi_B}{qN_a}} \text{ ....(3)}
\]

where \( V_{THO} \) is the classical threshold voltage estimate for the long channel transistor.

Due to the proximity effect, the drain electric field also starts influencing the height of the potential barrier at the source for the injection of free carriers into the channel (Drain Induced Barrier Lowering – DIBL). This effect is exacerbated by the fact that the electric fields in the device have increased over the years due to Generalized scaling behaviour. This manifests as a variation in threshold voltage as a function of drain bias. As a result, the drain electric field starts competing with the gate electrode to gain control over the channel conductivity. The transistor will no longer be an ideal gate controlled device. These effects make the transistor design a very challenging task at the nanoscale dimensions, for which many physics-based inputs are imperative.

\[
V_{TH} = V_{FB} + 2\Phi_B + \frac{Q_D}{C_\alpha} \left[ W_L H_L - 2x \frac{W_L \Delta L}{2} \right] \frac{1}{L_G W_L} \text{ ....(2)}
\]
1. NON CLASSICAL CMOS:

1.1 Channel and Source/Drain engineering:

The short channel effect should be controlled by screening the drain electric field and reducing the drain to source coupling volume. This requires an increase in the substrate doping concentration. However, a uniform increase in doping concentration also results in other detrimental effects such as mobility degradation due to impurity scattering, degradation of subthreshold slope, and increase in junction capacitance. This necessitates the engineering of the substrate doping concentration in the lateral and vertical direction. In the lateral direction, pocket halos are introduced at the edge of the source/drain regions to increase the doping concentration selectively. In the vertical direction, a super-steep retrograde profile is created, with a minimum doping in the channel region to minimize the carrier scattering (Fig. 4). In order to reduce the source/drain coupling, the junction depth should be scaled. But this results in issues such as higher resistance and possibility of metal contact spiking through the junction. This is circumvented by the creation of a deep source/drain region along with a very shallow extension (Fig. 4).

![Figure 4: Channel and Source drain engineering in Nano MOSFET](image)

1.2 High k-gate dielectric and metal gate electrode:

Fig. 5 (a) shows the SiO₂ gate oxide thickness scaling trend in CMOS technology. For the 65 nm technology node, the SiO₂ thickness is about 1 nm which is essentially two mono-layers of SiO₂ film. Fig 5 (b) shows the energy band diagram of the NMOS structure in the vertical direction for a positive applied bias. (This discussion holds good for the negative gate bias as well, except that the gate Fermi level, \( E_F \), will be above the substrate and the electrons will be tunnelling from the gate electrode). Typically the conduction across the SiO₂ insulator layer is negligible due to very large band offset (~3.1 eV) between the conduction band of gate/substrate and the conduction band of the oxide. However, for an ultra-thin gate oxide with \( T_\text{ox} < 5 \text{nm} \), carriers can quantum mechanically tunnel through the oxide and result in large gate leakage current. Furthermore, the tunnelling probability increases exponentially with decrease in \( T_\text{ox} \). Hence it is not possible to scale \( T_\text{ox} \) any further. This calls for replacement of SiO₂ with an alternate gate insulator which has a higher dielectric constant (\( k \)). The high-\( k \) dielectric of thickness of \( T_\text{hit} \) is equivalent to effective oxide thickness \( \text{EOT} = (3.9 / k) \times T_\text{hit} \), where SiO₂ dielectric constant is 3.9. Hence it is possible to use thicker insulator and reduce the gate tunnelling current, while maintaining capacitive coupling of the gate electric field to the channel that is equivalent to thinner oxide. In addition to high-\( k \), the insulator should also have other important properties such as very good interface with Si resulting in minimal interface traps, thermodynamic stability, large band gap and band offset with silicon. The search for a suitable high-\( k \) dielectric has been going on for more than a decade, and various metal oxides are being explored as high-\( k \) dielectrics [Locquet 2006, Singh 2003]. HfO₂ high-\( k \) gate dielectric has been introduced recently in the commercial 45 nm CMOS technology node [Mistry 2007].

One of the early problems with high-\( k \) dielectrics was the impact on the transport behaviour of carriers in the transistor channel. The low energy phonons corresponding to the dipole displacement in the high-\( k \) insulator would couple to the channel, resulting in remote phonon induced mobility degradation. The replacement of poly-silicon gate with metal-gate electrode was able to overcome this problem significantly due to image charge compensation. Hence all the MOSFETs with high-\( k \) dielectrics will invariably use metal gate electrode. Again, significant physics inputs to understand well the electron-phonon interactions.
helped to solve the problem. It is interesting to note that the need for metal gate electrode was also necessitated by the fact that the continuous reduction in gate length resulted in dramatic increase in gate resistance, affecting the transit time of the high frequency (GHz) signal along the width of the gate electrode.

Figure 5 : (a) Gate oxide thickness trend as a function of technology scaling, (b) Energy band diagram for NMOS with positive gate voltage, illustrating tunneling through gate oxide

1.3 Transport enhanced MOSFETs:

The increase in substrate doping concentration to suppress short channel effects has adversely affected the carrier mobility in the MOSFET channel due to increased impurity scattering. This problem can be overcome with the new class of non-classical CMOS transistors, namely the transport enhanced FETs. The technique relies on material engineering to enhance the channel mobility of the carriers. This class of devices includes strained-Silicon MOSFETs and hetero-epitaxially grown Germanium (Ge) or Gallium Arsenide (GaAs) channel MOSFETs on silicon substrate.

The strained-Silicon channel MOSFETs rely on a very well known phenomenon that the carrier mobility in silicon can be enhanced by introducing strain in silicon lattice. The tensile strain enhances the electron mobility and the compressive strain enhances the hole mobility. Several techniques have been employed for strain engineering in MOSFETs. The inter-atomic distance in Ge (2.45nm) is more than that of Si (2.36nm) and one technique exploits this difference to create tensile or compressive strain. A Si-Ge thin film is grown on silicon substrate by grading the Ge concentration from 0 to about 30%. This graded layer typically contains the defects and ensures that defect-free films can be grown on top. Then Si$_x$Ge$_{1-x}$ thin film is grown with an effective lattice constant higher than silicon. The thin silicon channel layer (about 10nm) is epitaxially grown on Si$_x$Ge$_{1-x}$, thus leading to a strained silicon channel. A very important consideration in creating this structure is to ensure that the strained silicon film is defect free, so that very high channel mobility can be obtained. A variation of this technique has been used for PMOS transistor to create compressive strain. The source/drain region is recessed into the substrate and the Si-Ge is selectively grown in the source/drain regions. This induces a compressive stress in the channel due to the lateral confinement from the two directions of the channel, leading to enhanced hole mobility. The other strain engineering technique relies on gate stack capping with appropriate material to induce stress in the underlying channel region. For example, capping the gate stack with Si$_x$N$_y$ can induce tensile stress and enhance the electron mobility. The isolation oxide in shallow trench region has also been utilized to induce strain in the channel region. Strained silicon channel MOSFETs have been successfully integrated with channel mobility improvement of more than 30% [Mistry 2007] in volume manufacturing. However, more radical techniques of transport enhancement will be required in future. Some of the potential candidates include Ge and GaAs MOSFETs on thin films grown hetero-epitaxially on silicon substrate. The electron mobility in Ge is more than twice that of silicon and the hole mobility is about 4 times that of silicon. Similarly the electron mobility in GaAs is about 6 times that of silicon. Historically, Ge and GaAs have never been amenable for building MOSFETs. While Si has an excellent insulator in terms of SiO$_x$, which results in an ideal interface with minimal trap density, Ge and GaAs did not have this advantage. But now that SiO$_x$ is being replaced with alternate high-$k$ gate dielectrics, similar dielectrics can potentially be employed with Ge and GaAs as well. There are recent reports with high quality germanium devices built
using high-k gate dielectrics [Krishnamohan 2006]. The major limitation at present is to have a reliable hetero-epitaxy process to obtain good quality channel material for wafer scale integration. The highly scaled MOSFETs are also expected to use metal source/drain junctions to replace diffused junctions. However, one of the major issues is the fact that the metal Fermi level gets pinned in the lower half of the bandgap for most of the semiconductors. As a result it is very difficult to form a good metal Schottky junction on p-type substrates to achieve source/drain regions for n-channel transistors. There have been recent attempts to de-pin the Fermi level to yield reliable Schottky contacts on both n- and p-type substrates [Arun 2010]. All these techniques will potentially lead to “enhanced silicon CMOS” technologies, while continuing to exploit the silicon infrastructure.

1.4 Multi Gate FETs:

The conventional technique of increasing the substrate doping concentration to suppress the short channel effect cannot be continued indefinitely. This is because the leakage at the drain/source to substrate junction due to tunneling will adversely affect the transistor performance. A more efficient technique to restore the gate control of the channel, without increasing the substrate doping, is very essential. Hence it is desirable to create a transistor with virtually intrinsic channel doping, at the same time ensuring adequate gate control of the channel. These requirements are the motivation for creating multi-gate FETs which include double-gate FET, tri-gate FET, Fin-FET and surround-gate nanowire FET [Shang 2006, Lee 2006, Colinge 2010]. By providing additional gates, the voltage on the gate can effectively couple to the channel, thereby enhancing the FET performance. FinFETs and nano-wire FETs with very good characteristics have been experimentally demonstrated. However, a manufacturable process integration still has a long way to go. All these multi-gate devices require an ultra-thin silicon channel region which should be reproduced and controlled efficiently.

2. CARBON BASED NANO STRUCTURED FETs:

Among the various non-silicon based device technologies, Carbon Nanotube (CNT) and Graphene transistors are considered to be the most important candidates. CNTs are essentially graphene sheet(s) rolled up into cylinders. They can be either single-walled with one graphene sheet rolled up or multi-walled with many sheets rolled up in to multiple coaxial cylinders separated by a distance equal to the inter-plane distance in graphite. The electronic property of the CNT can be either metallic and semiconducting depending on the atomic structure (roll-up mechanism), and the resulting chiral vector angle [Graham 2005, Broza 2010]. Depending on the formation, CNT can be in the configuration of armchair, zigzag and chiral CNT. The armchair CNTs are always metallic (the two basis vector coefficients $n$ and $m$ are equal), whereas the zigzag / chiral CNTs (chirality vector at an angle less than 30°) can either be semiconducting with $(n-m)/3$ not an integer or metallic with $(n-m)/3$ an integer. The electrons in CNTs are free to move along the axis of the nanotube. Hence the CNTs can display a mean free path as large as a few microns. In addition, current densities in the range of $10^{15}$ A/cm$^2$ can be achieved. This opens up the possibility of using CNTs as transistors and interconnects for highly scaled CMOS technologies. CNTs can be synthesized using processes such as arc discharge, laser ablation, chemical vapour deposition (CVD). Among these, CVD is more amenable for consideration in CMOS technology. However, CVD requires a metal catalyst such as iron (Fe) to seed and grow CNT. By using a photo-lithographically defined template of the catalyst, a regular array of CNTs can be achieved. While this is convenient to build interconnects, the process is not conducive for planar transistor integration. A vertical transistor concept has also been proposed, but is not compatible with the typical VLSI design framework at this time. There are demonstrations of planar CNT transistors by harvesting vertically grown CNT onto a substrate. But this process of harvesting tends to be statistically random and uncontrolled. Hence, scalability to achieve gigascale integration is non-trivial. Thus, CNTs seem to be more relevant for a variety of sensor applications [Sood 2003], rather than building blocks for large scale integrated circuits.

In the last decade, there has been a tremendous interest in Graphene, a monolayer of carbon atoms arranged in hexagonal lattice with honeycomb pattern [Novoselov 2004, Lin 2009, Schwierz 2010]. The greatest advantage for nanoelectronics...
applications is the fact that Graphene is amenable for planar technology. Graphene is typically prepared by mechanical exfoliation of monolayer of atoms from graphite. An alternate approach for wafer scale preparation is to grow on metal substrates using a CVD process and subsequently transfer onto an insulating substrate such as an oxidized silicon wafer. Graphene has a very unique band structure with linear energy-momentum dispersion (Fig. 6). This in turn gives rise to some unique properties for carrier transport in Graphene. For a suspended Graphene layer, a mobility value of $10^6$ cm$^2$/V-s has been reported [Geim 2010]. On the other hand, for exfoliated Graphene on SiO$_2$/Si substrate, mobility values in the range of 15,000 cm$^2$/V-s have been achieved [Chen, 2008]. Graphene grown on nickel substrate and subsequently transferred to other substrates has yielded mobility in the range of 3,700 cm$^2$/V-s [Kim 2009].

![Image of Graphene: Physical structure and Energy-band structure](image1)

![Image of BLG transistor with n Silicon source/drain region can potentially result in Ion/Ioff ratio in excess of 10,000](image2)

While Graphene has very high mobility, it also has zero bandgap, thus making it very difficult to get a well-behaved transistor. In particular, it will not be possible to turn off the MOSFET and hence the typical on current to off current ratio ($I_{on}/I_{off}$) has been less than 10. This should be contrasted with a typical silicon MOSFET which has $I_{on}/I_{off}$ greater than 10,000. Several techniques have been proposed to open the bandgap in Graphene. It has been demonstrated, both theoretically and experimentally, that Graphene Nanoribbons (GNR) show a bandgap which is inversely proportional to their width. GNRs with about 20 nm width have bandgaps in the range of 100 meV. But it is very difficult to obtain GNRs with well defined edges. An alternate technique to open the band gap is to use bilayer Graphene (BLG), with an asymmetric bias applied in the direction perpendicular to their plane. Typical bandgaps of 200 meV are obtained for fields in the range of $10^7$ V/cm. The MOSFET on BLG Graphene have resulted in $I_{on}/I_{off}$ of about 100. This is still inadequate for typical digital CMOS applications. However, these devices are attractive for RF CMOS applications, since unity gain cut-off frequency ($f_t$) of more than 100 GHz has been demonstrated on such devices [Lin 2010]. A recent simulation study has used silicon source/drain junctions in conjunction with Graphene channel to enhance the $I_{on}/I_{off}$ ratio [Majumdar 2010]. In typical Graphene transistors with metal source/drain junctions, the off current results because of hole tunnelling from the drain region into the channel. This increases with increasing drain bias, thus degrading the $I_{on}/I_{off}$ ratio further at higher drain bias conditions. By using silicon source/drain junctions, the tunnelling component of hole current can be completely shut off. This is illustrated in Fig. 7. An $I_{on}/I_{off}$ ratio of more than 10,000 has been demonstrated. Since Graphene transistors have favourable electrostatics to scale down to sub-10 nm gate length, due to ultra-thin channel region, the short channel effects will be insignificant. Hence, Graphene transistors are potential candidates for post-silicon device options, provided high $I_{on}/I_{off}$ ratio can be achieved with wafer scale processing capability. The development of next generation Graphene transistors, with manufacturable process flow is a potential area for physicists, chemists and engineers to collaborate.
3. FLASH MEMORY TECHNOLOGY

Memories have been an important technology driver in electronics ever since Intel introduced its 1 kilobit memory – the first ever MOS circuit – in 1970. Today, one can get a 64 Gbit flash memory chip, which represents an enormous increase in density and capability. Memory technology continues to be innovative, coming up with new structures and methods to store information, all entailing new physics.

Of all the different memory types and architectures, the one which is growing the fastest today is the “flash” memory [Bez 2003], which will form the subject of this section. Flash memories are a type of non-volatile silicon-based memory, in which the basic cell which stores the 0 or 1 is a modified MOS transistor. Two relatively new flash memory cell structures, called charge trap cells, are shown in Fig 8 (a) and (b). The structure in Fig 8 (a) is the SONOS (silicon-oxide-nitride-oxide-silicon) device [White 2000], and that in Fig. 8 (b) is the metal nanocrystal device [Liu 2002]. Both the devices have nano-scale structures which are critical to their operation.

![Figure 8: Structures of the (a) SONOS flash memory and (b) Metal nanocrystal flash memo](image)

The SONOS device is like a MOS transistor, except that the gate insulator is replaced by a stack of silicon dioxide (O), silicon nitride (N) and silicon dioxide (O). The bottom silicon dioxide is of tunnelling thickness, typically about 2 nm. The nitride layer has many electron traps, and charge can be stored in these traps. The top (or blocking) oxide is relatively thick to prevent tunnelling to or from the top gate. The memory cell gets “programmed” by applying a large positive voltage to the gate, which produces a large field in the bottom (or tunnelling) oxide, which in turn results in electrons being injected into the insulator stack by Fowler-Norheim (or sometimes direct) tunnelling. The oxide is very trap-free, and many of the injected electrons end up getting trapped in the nitride layer. Even after the positive voltage is removed, the charge is retained in the deep electron traps in the nitride, thus making the storage non-volatile. The presence of negative charge in the insulator stack increases the threshold voltage of the transistor, which therefore cannot be turned on during normal application of the “read” voltage to the gate. The charge can be removed (erased) from the nitride by applying a large negative voltage, under which the electrons tunnel back to the substrate, or holes are injected from the substrate to neutralize the electrons. This is a fairly complicated processes, whose physics needs to be better understood. The band diagrams of the SONOS structure during program and erase operations is shown in Figs. 9 (a) and (b). The cyclable shift in the threshold voltage is depicted in Fig. 10, which shows the $I_v-V_c$ characteristic of the cell after program and erase. Note that under the typical “read voltage”, current can flow in the uncharged state, but no current can flow in the charged state, thus enabling a distinction between a 1 and a 0. The read voltage is quite low, and no significant program and erase occurs during this phase. However, the charge does eventually leak out; the time during which it can be safely stored is called the retention time.
builds, the rate of build up decreases. The solution of Eq. (8) is approximately

\[ n_r \approx \frac{1}{m} \ln(t) + B \]  

which is the required log-time dependence. Note that the number of trapped charges \( n_r \) is directly proportional to the threshold voltage shift, so this equation predicts that the threshold voltage increases as log (t), as seen in Fig. 11. Based on similar physical considerations, one can say the following: (1) Programming times can be reduced by increasing the program voltage or decreasing the bottom oxide thickness, but the latter will have the negative consequence of also reducing the retention times (2) Retention times can be increased if the silicon nitride is engineered to have deep electron traps [Sandhya 2009] (3) Top blocking oxide should be thick to prevent back injection of holes or electrons (as a consequence the top oxide is often Al O or a high-k dielectric instead of silicon dioxide).

The nanocrystal flash memory (Fig. 8 b) functions in a similar way, except that the charge is stored not in traps in the nitride, but rather in 2-3 nm diameter nanocrystals of metal (often platinum) embedded in the silicon dioxide. These nanocrystals are again located within tunnelling distance of the substrate, and electrons can tunnel back and forth, thus programming and erasing the device. Metal nanocrystal flash memories have the advantage over SONOS that they can potentially store more charge and have better controllability, if the difficult technological problem of how to get uniform nanocrystal deposition can
be overcome. Though the operation of the nanocrystal flash memory is qualitatively similar, it is analytically and even numerically difficult to solve, because of the inherently 3-dimensional nature of the problem. The metal nanocrystals should not be too close together, else they will be able to share charge easily by inter-dot tunnelling, and as a consequence, the presence of a single leakage path will empty out all the stored charge. On the other hand, the nanocrystals should not be too far apart, as they would not then be able to effectively turn off the channel in the substrate. One way to bypass this dilemma is to have the nanocrystals in two layers instead of one [Singh 2008].

Typical program times of the cell are quite large – of the order of tens of microseconds. Since each cell has to be individually programmed, writing 1 Mbit of information can take several seconds. This is rather slow compared with static and dynamic memories, which are, however, volatile, and cannot retain information after the power is turned off. Erasing the information can be done not just one cell at a time, but for a whole block, so several Mbits of information can be erased in a few microseconds – “in a flash”, hence the name. (This asymmetry in the program and erase times is easily noticeable when using a flash memory stick.) Typical retention times are of the order of years, and depend on various parameters like temperature, depth of electron traps in the nitride (for SONOS), type of metal used (for nanocrystal), thickness and quality of underlying silicon oxide, etc. Finally the number of program/erase cycles is finite, usually about $10^5$, limited by trap creation in the oxide layers during the high-field program and erase modes.

There are many underlying physics-based processes which need to be understood and modelled to analyze and predict the behaviour of the flash memory devices. These processes include: Fowler-Nordheim tunnelling, direct tunnelling, trap-to-band tunnelling, charge transport in silicon nitride, electron (and hole) trapping dynamics, recombination of trapped charges with free carriers, quantum confinement effects, and trap creation processes under high applied fields. The design of better flash memories thus represents an opportunity for physicists and device engineers to collaborate fruitfully.

4. NANOELECTRONICS INITIATIVES IN INDIA AND THE INDIAN NANOELECTRONICS USERS PROGRAMME

Over the last 5 years, there has been a significant impetus given to Nanoelectronics in India. In 2003, the Principal Scientific Adviser to the Government of India, Dr. R. Chidambaram, led a country-wide discussion on how to initiate a nanoelectronics activity in India. It was felt that though India had been a bystander in the microelectronics revolution that swept across East Asia in the 1990s, the time was now appropriate to embark on nanofabrication activities to complement the strong VLSI design and software capability which had developed in India. Further, it emerged from the discussions that it would be better to set up only one or two well-endowed nanofabrication facilities rather than spread the funding thinly across many organizations, and further that the facilities should be created at existing academic institutions, which would directly contribute to manpower development in this new area.
As a result of this initiative, the Department of Information Technology (the erstwhile Department of Electronics) set up in 2005 two tightly coupled “Centres of Excellence in Nanoelectronics” (CEN) at the Indian Institute of Science (IISc) and the Indian Institute of Technology Bombay (IITB) through the funding of a single joint project operating at these two institutions. The work at these two Centres was planned to be complementary, with IISc focusing on material-oriented “bottom-up” approaches, and IITB on device-oriented “top-down” approaches. These approaches were consistent with the existing strengths at the two institutes, and also broadly reflected the science versus technology emphases of the two institutes.

These two Centres have now been functioning for 5 years. Both have set up excellent nanofabrication facilities, and have engaged in a variety of activities in different areas of nanoelectronics. Views of some of the facilities at IISc and IITB are shown in Fig. 12 (a) and Fig. 12 (b) respectively. The funding from DIT has attracted significant funding and equipment donation from industry. For example, Applied Materials Inc, donated IITB three cluster tools for CMOS fabrication, and Agilent has donated IISc two tools for characterization. In addition other funding agencies in the country have also complemented DIT funding. For example IITB has received major funding from MNRE, whereas IISc has received significant funding from DST and NPMASS. Furthermore, both institutes contributed internal funding to set up the laboratories, clean rooms and infrastructural facilities.

Another major initiative, intimately connected to the Centres of Excellence in Nanoelectronics, was the launching of the Indian Nanoelectronics Users Programme (INUP). The purpose of INUP, which was also funded by DIT as a joint project at IISc and IITB in 2008, was to make available the facilities created at the two CENs to all academic (and other) users across the country who wished to do nanofabrication. Indeed, the idea of INUP was conceived simultaneously with the CENs. It was felt that concentrating the funding for nanofabrication facilities in only a couple of places would be justifiable if there was a satellite programme which ensured easy access to these facilities for others in the country who needed to use them. INUP has run several “orientation” and “hands-on training” workshops in the last 2 years, which have attracted over 500 participants who are all potential users of the CEN facilities. So far, over 150 users from about 60 organizations have come to IITB or IISc to use the facilities. Most of the users are research students and faculty from academic institutions, but there have also been users from industry and R&D laboratories. Users from academia see no cost to themselves (their work is supported by the DIT INUP funding), while users from industry and R&D laboratories are charged on an hourly basis for use of different equipment. Several publications and conference papers (about 20 in the 2 years that the programme has been operating) have resulted from work done by the users under INUP. Details on how to access the nanofabrication facilities at the CENs are available at www.inup.org.in.

5. CONCLUSIONS:

In this paper, we have presented an overview of the current state-of-the-art in Nanoelectronics, with an emphasis on logic and storage applications. The issues in developing high-performance nanoscale transistors are elaborated upon, and different transistor design approaches are presented to overcome the problems of scaling. The significance of nanostructured transistors based on CNT and Graphene is also discussed. The evolution of Flash memory technology is discussed along with the future directions in scaling the memory technology. We have described a major Nanoelectronics initiative in India, launched by DIT, resulting in two Centres of Excellence in Nanoelectronics at IISc and IIT Bombay. The unique outreach program, “Indian Nanoelectronics Users Program” has been successful in empowering researchers in the country, who did not earlier have access to the expensive infrastructure, by facilitating them to use the nanofabrication facilities created at IISc and IIT Bombay.

REFERENCES: