Lecture # 3

E3-238 : Analog VLSI Circuits

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| L-3 | 17-8-05 | SPICE simulator, Transistor models, BSIM3 models, Model extraction, Models for: Vt, I-V, Capacitance, Substrate current, S/D parasitics, Temp dependence, NQS effect, Noise, RF Modeling, *Gate leakage* |
Device Models

- Device models are the links between Technology and Design
- Device models abstract the complete behaviour of the device

Depending on the abstraction accuracy requirement, models with different complexity may be used
Types of Models

Numerical model:
Solve the basic governing equations for the device using numerical techniques (Poisson, Continuity, Transport equations)
Most accurate, but computationally inefficient

Table look up model:
Construct a look up table from the measured results and interpolate the device behaviour
Simple and no equations to be solved, table size grows exponentially with device complexity and the desired accuracy

Analytical (Compact) model:
Physics based analytical equations describe the device behaviour
A set of model equations and a set of model parameters
“Compact” and used by all the circuit simulators
Simulation Program with Integrated Circuit Emphasis (SPICE)

SPICE engine solves nodal equations constrained by KVL & KCL

Netlist

Model file

Values for the parameters

Model equations are Subroutines in SPICE

I/P & Type of analysis

DC, AC Transient

Nodes Elements Connectivity

Circuit behaviour

First SPICE program was released by UC Berkeley in 1973
All the commercial versions are based on this general framework
MOSFET Model Evolution

• First generation: (1968) Level 1 Level 2, Level 3
  Very simple device equations
  Valid mostly for large devices

• Second generation: (1987) BSIM1, BSIM 2, Level 28 (Hspice)
  More rigorous, but very empirical
  Emphasis on curve fitting the experimental device behaviour,
  rather than incorporate underlying device physics

• Third generation: (1995) BSIM3
  Physics based, with a few empirical parameters
  Emphasis on developing single equation model rather
  than piecewise model
Level 1

• First MOSFET model released in 1968

• Valid for long channel uniformly doped devices (used in 1970s)

• Very small set of parameters (10)

• Very simple quadratic behaviour of transistor

* A typical Level 1 parameter file *

```
.model Name_model NMOS Level=1
+TPG=1 TOX=10-7 NSUB=1E16 XJ=1E-6
+ UO=600 VTO=1.5 LAMBDA=0.01
+CGSO=1E-16 CGDO=1E-16 CGBO=1E-17
```
BSIM3V3.2


• BSIM3V3 was selected as the first Compact model for industry standardization by the Compact Modeling Council (1996)

• BSIM3V3.2 (1998) is popularly used in circuit simulators Level = 8 in spice3f5, Level=49 Hspice, Level=53 in Eldo

• Uses single equation approach with enhanced modeling of small dimension transistors

• First comprehensive model for analog & RF with continuity in transistor parameters and their derivatives across different regions of transistor operation
BSIM3V3.1 for a particular 0.35µm technology

• A typical BSIM3V3.2 model has more than 150 model parameters
Vth Model

\[
V_{th} = V_{th0\alpha x} + K_{1\alpha x} \sqrt{\Phi_s - V_{bseff}} - K_{2\alpha x} V_{bseff}
\]

\[
+ K_{1\alpha x} \left( \sqrt{1 + \frac{N\deltax}{L_{eff}}} - 1 \right) \sqrt{\Phi_s + \left( K_3 + K_3 b \right) V_{bseff}} \frac{T_{\alpha x}}{W_{eff}^* + W_0} \Phi_s
\]

\[
- D_{VT0} \left( \exp \left( - D_{VT1} \frac{W_{eff} L_{eff}}{2 l_{bv}} \right) + 2 \exp \left( - D_{VT1} \frac{W_{eff} L_{eff}}{l_{bv}} \right) \right) (V_{bl} - \Phi_s)
\]

\[
- D_{VT0} \left( \exp \left( - D_{VT1} \frac{L_{eff}}{2 l_t} \right) + 2 \exp \left( - D_{VT1} \frac{L_{eff}}{l_t} \right) \right) (V_{bl} - \Phi_s)
\]

\[
- \left( \exp \left( - D_{sub} \frac{L_{eff}}{2 l_{lo}} \right) + 2 \exp \left( - D_{sub} \frac{L_{eff}}{l_{lo}} \right) \right) \left( E_{fao} + E_{tab} V_{bseff} \right) V_{ds}
\]
Non uniform vertical doping

\[ V_{th} = V_{FB} + \Phi_s + \gamma \sqrt{\Phi_s - V_{bs}} = V_{T_{ideal}} + \gamma \left( \sqrt{\Phi_s - V_{bs}} - \sqrt{\Phi_s} \right) \]

\[ V_{th} = V_{th0_{ox}} + K_{1_{ox}} \cdot \sqrt{\Phi_s - V_{b_{seff}}} - K_{2_{ox}} V_{b_{seff}} \]

\[ V_{th0_{ox}} = V_{th0} - K_1 \cdot \sqrt{\Phi_s} \]

\[ K_{1_{ox}} = K_1 \cdot \frac{T_{ox}}{T_{ox_{nm}}} \]

\[ K_{2_{ox}} = K_2 \cdot \frac{T_{ox}}{T_{ox_{nm}}} \]

V_{b_{seff}} is “smoothened” effective V_{bs} value
Non uniform lateral doping (halo)

\[ N(x) \]

\[ N_{pocket} \quad N_a \quad N_{pocket} \]

\( L_x \quad L_x \quad X \)

\[ + K_{\text{lo}} \left( \sqrt{1 + \frac{N_{lx}}{L_{\text{eff}}}} - 1 \right) \sqrt{\Phi_s} \cdot \]

\[ L_{\text{eff}} = L_{\text{drawn}} - 2dL \]

\[ dL = L_{\text{int}} + \frac{L_l}{L_{L\ln}} + \frac{L_w}{W_{L\ln}} + \frac{L_{wl}}{L_{L\ln}W_{L\ln}} \]

Nlx is the excess doping in the pocket halo regions

LL, LW, LWL are typically zero
Narrow width effect

\[
\left( K_3 + K_{3b} V_{b\text{seff}} \right) \frac{T_{ox}}{W_{\text{eff}}' + W_0} \Phi_s
\]

\[
W_{\text{eff}}' = W_{\text{drawn}} - 2dW'
\]

\[
dW' = W_{\text{int}} + \frac{W_i}{L^{W_{\text{ln}}}} + \frac{W_w}{W^{W_{\text{wn}}}} + \frac{W_{w_l}}{L^{W_{\text{ln}}W^{W_{\text{wn}}}}}
\]

\[
W_{\text{eff}} = W_{\text{drawn}} - 2dW
\]

\[
dW = dW' + dW_g V_{g\text{seff}} + dW_b \left( \sqrt{\Phi_s - V_{b\text{seff}}} - \sqrt{\Phi_s} \right)
\]

\[
V_{b\text{seff}} = V_{bc} + 0.5 \left[ V_{bs} - V_{bc} - \delta_1 + \sqrt{(V_{bs} - V_{bc} - \delta_1)^2 - 4\delta_1 V_{bc}} \right]
\]

\[
V_{bc} = 0.9 \left( \Phi_s - \frac{K_1^2}{4K_2^2} \right)
\]

- Allows the modeling of substrate bias dependence of NWE
- \( V_{b\text{seff}} \) is the smoothened \( V_{bs} \) with \( V_{bc} \) equal to maximum allowable \( V_{bs} \) for the condition \( dV_{th}/dV_{bs} = 0 \)
Short channel effect: Charge sharing

\[-D_{VT0w} \left\{ \exp \left( -D_{VTn} \frac{W_{eff} L_{eff}}{2l_{tw}} \right) + 2 \exp \left( -D_{VTn} \frac{W_{eff} L_{eff}}{l_{tw}} \right) \right\} (V_{bi} - \Phi_s)\]

\[-D_{VT0} \left\{ \exp \left( -D_{VTn} \frac{L_{eff}}{2l_t} \right) + 2 \exp \left( -D_{VTn} \frac{L_{eff}}{l_t} \right) \right\} (V_{bi} - \Phi_s)\]

\[l_t = \sqrt{\varepsilon s_i X_{dep} / C_{ox} \left( 1 + D_{VT2} V_{bseff} \right)}\]

\[l_{tw} = \sqrt{\varepsilon s_i X_{dep} / C_{ox} \left( 1 + D_{VT2w} V_{bseff} \right)}\]

- $V_t$ reduction due to the charge sharing is modeled as a function of $L_{eff}$

- Lower the value of $L_{eff}$, larger is $V_t$ reduction due to charge sharing

It and $l_{tw}$ are characteristic lengths
Computed from model parameters
Short channel effect : DIBL

\[-\left( \exp\left(-D_{sub} \frac{L_{eff}}{2l_{to}} \right) + 2\exp\left(-D_{sub} \frac{L_{eff}}{l_{to}} \right) \right) \left( E_{ta0} + E_{tab} V_{bseff} \right) V_{ds} \]

\[l_{to} = \sqrt{\varepsilon_{st} X_{dep0} / C_{ox}} \]

\(l_{to}\) is characteristic length computed internally

• The effect of body bias on DIBL is also captured
Model versus Experimental data

A note on VTH0 in the model file:

Extracted for the long and wide device with Vds= 0.05V and extrapolation
From the peak gm point on the Id-Vg characteristics:

VTH0 = Vgs(@ Id=0) – 0.5Vds
**Effective \( V_{gs-Vt} \)**

continuity in channel using \( V_{gsteff} \), \( Q_{ch}=C_{ox}.V_{gsteff} \)

\[
V_{gsteff} = \frac{2 \, n \, v_t \ln \left[ 1 + \exp\left( \frac{V_{gs} - V_{th}}{2 \, n \, v_t} \right) \right]}{1 + 2 \, n \, C_{ox} \sqrt{\frac{2 \Phi_s}{\varepsilon_{st} N_{ch}}} \exp\left( -\frac{V_{gs} - V_{th} - 2 V_{off}}{2 \, n \, v_t} \right)}
\]

\[
n = 1 + N_{factor} \frac{C_d}{C_{ox}} + \frac{C_{dsc} + C_{dscd} V_{ds} + C_{dscb} V_{bsteff}}{C_{ox}} \left( \exp\left( -\frac{L_{eff}}{2l_t} \right) + 2 \exp\left( -\frac{D_{VT} L_{eff}}{l_t} \right) \right) + \frac{C_{it}}{C_{ox}}
\]

\( V_{off} \) is the offset parameter which fits the subthreshold region

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Polysilicon gate depletion effect

- This effect is very specific to the technology

- The following correction is applied only if required

\[
V_{gs\_eff} = V_{FB} + \Phi_s + \frac{q\varepsilon_{si} N_{gate} T_{ox}^2}{\varepsilon_{ox}^2} \left( \frac{2\varepsilon_{ox}^2 (V_{gs} - V_{FB} - \Phi_s)}{q\varepsilon_{si} N_{gate} T_{ox}^2} \right) - 1
\]

Vgs in model equations replaced with Vgs_eff

The effective inversion charge decreases due to voltage drop across poly
Effective Vds

Vdseff is introduced for continuity in Ids and its derivative at Vdsat,

\[
V_{dseff} = V_{dsat} - \frac{1}{2} \left( V_{dsat} - V_{ds} - \delta + \sqrt{(V_{dsat} - V_{ds} - \delta)^2 + 4\delta V_{dsat}} \right)
\]

\[
V_{dsat} = \frac{E_{sat} \cdot L_{eff} (V_{gsteff} + 2V_t)}{A_{bulk} E_{sat} \cdot L_{eff} + (V_{gsteff} + 2V_t)}
\]
Mobility model

Accounts for mobility degradation with vertical field

\[ \text{mobMod} = 1, 2, 3 \text{ options:} \]

\[
\mu_{\text{eff}} = \frac{\mu_o}{1 + (U_a + U_c V_{b\text{seff}})(\frac{V_{g\text{steff}} + 2V_{\text{th}}}{T_{\text{OX}}}) + U_b(\frac{V_{g\text{steff}} + 2V_{\text{th}}}{T_{\text{OX}}})^2}
\]

\[
\mu_{\text{eff}} = \frac{\mu_o}{1 + (U_a + U_c V_{b\text{seff}})(\frac{V_{g\text{steff}}}{T_{\text{OX}}}) + U_b(\frac{V_{g\text{steff}}}{T_{\text{OX}}})^2}
\]

\[
\mu_{\text{eff}} = \frac{\mu_o}{1 + [U_a(\frac{V_{g\text{steff}} + 2V_{\text{th}}}{T_{\text{OX}}}) + U_b(\frac{V_{g\text{steff}} + 2V_{\text{th}}}{T_{\text{OX}}})^2](1 + U_c V_{b\text{seff}})}
\]
Drain current model

\[
I_{ds} = \frac{I_{dso(Vdseff)}}{1 + \frac{R_{dsI_{dso(Vdseff)}}}{V_{dseff}}} \left(1 + \frac{V_{ds} - V_{dseff}}{V_{A}}\right) \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ASCBE}}\right)
\]

\[
I_{dso} = \frac{W_{eff} \mu_{eff} C_{ox} V_{gseff} (1 - A_{bulk} \frac{V_{dseff}}{2(V_{gseff} + 2V_{t})})}{L_{eff} [1 + V_{dseff} / (E_{satL_{eff}})]} V_{dseff}
\]

\[
V_{A} = V_{Asat} + \left(1 + \frac{P_{vag} V_{gseff}}{E_{satL_{eff}}}(\frac{1}{V_{ACLML}} + \frac{1}{V_{ADIBLC}})\right)^{-1}
\]

\[
V_{ACLML} = ... \quad V_{ADIBLC} = ...
\]

\[
R_{ds} = \frac{R_{dsw} \left(1 + P_{rwa} V_{gseff} + P_{rwb} \left(\sqrt{\Phi_{s} - V_{bseff}} - \sqrt{\Phi_{s}}\right)\right)}{(10^{6} W_{eff})^{w_{r}}}
\]
Substrate current model

Substrate current depends on impact ionization coefficient

\[
I_{\text{sub}} = \alpha_0 + \alpha_1 \cdot \frac{L_{\text{eff}}}{L_{\text{eff}}} (V_{ds} - V_{dseff}) \exp\left(-\frac{\beta_0}{V_{ds} - V_{dseff}}\right) \frac{I_{ds0}}{R_{ds}I_{ds0}} \left(1 + \frac{V_{ds} - V_{dseff}}{V_A}\right)
\]

The model tracks the typical impact ionization behaviour
Capacitance model

The capacitance between two nodes is defined as:

\[ C_{ij} = \frac{\partial Q_i}{\partial V_j} \quad i,j=D,G,S,B \]

For a two terminal capacitor, capacitance reciprocity is valid

\[ C_{ij} = \frac{\partial Q_i}{\partial V_j} = -\frac{\partial Q_i}{\partial V_j} = \frac{\partial Q_j}{\partial V_i} = C_{ji} \]

- Meyer model is the simplest capacitance model used in early simulators, which treats MOSFET capacitances as reciprocal
- Unrealistic result of charge build-up due to charge non-conservation

- **Extrinsic capacitances are reciprocal and should also be added to intrinsic capacitances**
Trans-capacitance

However, for 4 terminal MOSFET, capacitance reciprocity violates charge neutrality condition

\[ Q_G + Q_D + Q_S + Q_B = 0 \]

\[ \frac{\partial Q_G}{\partial V_{GS}} + \frac{\partial Q_D}{\partial V_{GS}} + \frac{\partial Q_S}{\partial V_{GS}} + \frac{\partial Q_B}{\partial V_{GS}} = 0 \]

If \( C_{GS} = C_{SG} \)

\[ \frac{\partial Q_D}{\partial V_{GS}} + \frac{\partial Q_B}{\partial V_{GS}} = 0 \]

In inversion we know that, \[ \frac{\partial Q_B}{\partial V_{GS}} = 0 \]

This results in an incorrect conclusion, \[ \frac{\partial Q_D}{\partial V_{GS}} = 0 \]

Hence MOSFET capacitances should really be called transcapacitance
And the capacitance reciprocity is not valid for MOSFET
Charge versus terminal voltage model

\[ Q_i = f(V_G, V_D, V_S, V_B) \quad i = G, D, S, B \]

16 trans-capacitances are possible, of which only 12 are independent

\[ C_{GG} = -(C_{SG} + C_{DG} + C_{BG}) \ldots \text{and so on} \]

The capacitance model in BSIM3 is essentially charge-voltage Relationship (capMod=0,1 piece-wise 3,4 single equation with 4 accounting for channel quantization as well)

When the voltage state variable is obtained during SPICE run, charge is computed and hence capacitance is calculated

This is in contrast to obtaining the charge by integrating C(V)\*V
Charge Partitioning

In strong inversion and saturation region, the channel charge has to be partitioned into source and drain charge

\[ Q_S + Q_D = Q_{inv} \]

BSIM3 gives 3 options of charge partitioning

\[ D/S = 0/100 \ (X_{PART}>0.5), \ 50/50 \ (X_{PART}=0.5), \ and \ 40/60 \ (X_{PART}<0.5), \]

The exact partitioning is a very complex function, however, 40/60 is reasonably accurate

It would still give unrealistic negative spike in Id when Vgs is quickly ramped across Vth (NQS effect is operating)
Choice of devices for measurements

Also include minimum L & W device

Measurements: I-V and C-V
Extraction procedure

Extraction and optimization programs are available from different vendors

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Summary

• BSIM3v3.2 is the most widely used transistor model

• Single equation and continuity of parameters across the different regions of operations is ensured

• Capacitance reciprocity does not apply in MOSFETs; the capacitance should be referred to as transcapacitance

• Temperature dependence is captured for temperature sensitive parameters such as mobility, threshold voltage, mobility etc.

• Parasitic junction diode and capacitance model completes the I-V and C-V model construction
References

1. MOSFET Modeling with SPICE, Daniel Foty, *Prentic Hall*


3. BSIM web site at UC Berkeley

4. http://www.mosis.org for typical level 49 models on a variety of technologies