

Planar Inter Digital Capacitors on Printed Circuit Board

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Abstract— Coplanar wave guide (CPW) inter digital capacitor (IDC) configurations on printed circuit board (PCB) and parametric variations over frequency are studied by simulation using ADS Momentum. The structures are fabricated in printed circuit board using PCB fabrication techniques. The scattering parameters of the structure are measured using vector network analyzer (VNA). The capacitance is estimated in both case using an approximate circuit model and simulation. A Comparative study of the simulation performance with measured results conducted.

Index Terms— Coplanar wave guide, inter digital capacitor on PCB, ADS Momentum

I. INTRODUCTION

INTER digital capacitors on coplanar wave guide find application in filter circuits, hybrid couplers, dc blocking circuits, tuning elements in impedance matching network, RF bypass circuits and slow wave structures [1]. The inter digital capacitors on coplanar wave guide and their full wave equivalent circuits have been studied [2],[3]. The fabrication of series and shunt type inter digital capacitor on coplanar wave guide is very easy, so it is very convenient to use this capacitors for periodic loading in planar transmission lines. In this paper, we made an attempt to study the performance of inter digital capacitors on printed circuit board. The structures are simulated using software ADS momentum, an approximate circuit equivalent model is used formulated to emulate the capacitance values from the simulation results. The structures are fabricated in printed circuit board. A Comparative study of the simulation performance with measured results conducted

II. COPLANAR WAVE GUIDES

A micro strip line has the disadvantages of multi mode propagation and problem of realization of shunt components, and these problems were solved in a coplanar wave guide. A coplanar wave guide is a planar structure on a dielectric substrate consists of a center strip conductor with semi infinite ground line, and these structures supports propagation of quasi-TEM mode [1].

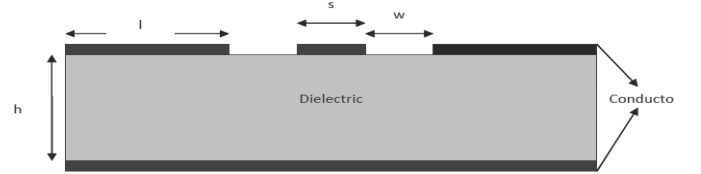


Fig. 1 Conductor backed CPW

Coplanar wave guides are classified as conventional CPW (infinite dielectric CPW) and conductor backed CPW (finite dielectric CPW). Figure 1 shows the structure of a conductor backed CPW. The structure has a dielectric medium bounded by two conductive layers. The top conductive layer forms the planar wave guide structure and the bottom conductor act as a ground line. The effective dielectric constant of the can be formulated based on a quasi-static conformal mapping techniques [4]. The effective dielectric constant ϵ_{eff} is given by

$$\epsilon_{eff} = 1 + \frac{\epsilon_r - 1}{2} * \frac{K(k'_0)K(k_1)}{K(k_0)K(k'_1)}$$

And the characteristic impedance

$$Z_0 = \frac{30 * \pi * K(k'_0)}{\sqrt{\epsilon_{eff}} K(k_0)}$$

Where

$$k_0 = \frac{s}{s + 2w}$$

$$k'_n = \sqrt{1 - (k_n)^2}$$

$$k_1 = \frac{\text{Sinh}\left(\frac{\pi * s}{4h}\right)}{\text{Sinh}\left(\frac{\pi(s + 2w)}{4h}\right)}$$

So the characteristic impedance of the wave guide is a function of the width of the strip, width of the slot, dielectric constant and height of the dielectric material. A conventional coplanar wave guide has a substrate dielectric medium and on top of the dielectric substrate the wave guide structure is formed. Fig. 2 show the simple structure of a conventional coplanar wave guide

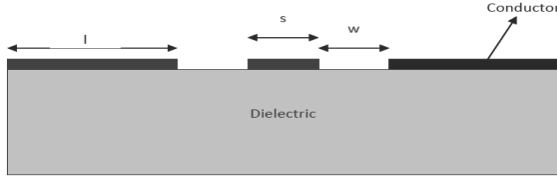


Fig. 2 Conventional Coplanar Wave Guide.

The dielectric medium is not terminated by the ground plane, so it is considered as an infinite dielectric medium. The characteristic impedance and the effective dielectric constant of such a medium can be expressed as $\epsilon_{eff} = 1 + \frac{\epsilon_r - 1}{2}$. The characteristic equation is the

same of the above case. So the design of a conventional coplanar wave guide is simple than the conductor backed coplanar wave guide, because the characteristic impedance of the wave guide is a function of the width of the strip, width of the slot, and dielectric constant and not a function of height of the dielectric material. So the conventional coplanar wave guide structure was used.

III. INTER DIGITAL CAPACITOR

The simple method of realizing a capacitor in a coplanar wave guide is by providing a slot in the middle of the conductive strip. This will act like a parallel plate capacitor, the capacitance of a parallel plate capacitor is a direct function of the cross sectional area of the conductor, cross sectional area of the strip line of the coplanar wave guide is very small, so it is not possible to realize required value of capacitance using this method. The area of interaction can be improved by incorporating a comb structured electrode in between the strip. Such structure is called inert digital capacitor structure and it is shown in figure 3

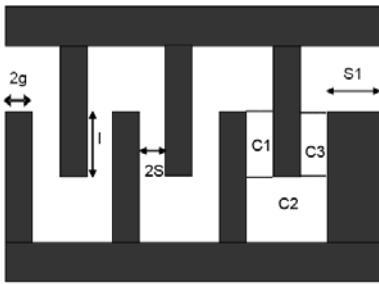


Fig. 3 IDC structure

The effective capacitance of the configuration can be estimated the using conformal mapping method. The effective capacitance can be contributed by combination of three capacitive structures shown in figure. The capacitance of the structures can be estimated using the equations [6] stated below.

$$c_1 = \epsilon_0 \epsilon_{eff} * \frac{K(k'_{01})}{K(k_{01})} * l$$

Where

$$k_{01} = \sqrt{1 - \left(\frac{g}{g+s}\right)^2}$$

$$c_2 = 2\epsilon_0 \epsilon_{eff} * \frac{K(k_{01})}{K(k'_{01})} * l_{ext}$$

Where

$$l_{ext} \approx \frac{l}{4}$$

$$c_3 = 4\epsilon_0 \epsilon_{eff} * \frac{K(k'_{02})}{K(k_{02})} * l$$

$$k_{02} = \sqrt{\frac{S1 * S}{(2g + S) * (2g + S1)}}$$

$$C = (n-3)C_1 + (n-1)C_2 + 2C_3$$

IV. CAPACITIVE STRUCTURES

A. Series capacitor

The equivalent circuit of a series capacitor on CPW is shown in figure 4. The capacitance of this configuration can be de-emulated from simulation scattering parameters. The structure with and without the capacitive structure is simulated. The S parameters obtained From simulation is converted to Z and Y parameters using the functions "stoz(S,Z0)" and "stoy(s,Z0)" available in ADS. Then the extraction of the capacitance is done in ADS using function equations.

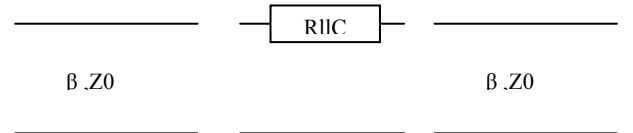


Fig. 4 Equivalent circuit of series capacitor on CPW

$$Z_C = Z_{Total} - Z_{Line}$$

$$Z_C = \frac{R}{1 + j\omega RC}$$

Z_C is in the form of $a+jb$ so

$$Z_c = \frac{R(1 - jwRC)}{1 + (wRC)^2}$$

$$a(1 + (wRC)^2) = R$$

$$b(1 + (wRC)^2) = wRC$$

$$bR - awRC = 0$$

$$C = \frac{b}{aw}$$

B. Shunt Capacitor

. As stated above the capacitance of this configuration can be demulated from simulation scattering parameters. The equivalent circuit for analytical method is shown in Figure7 and a modified one is in Fig. 5.

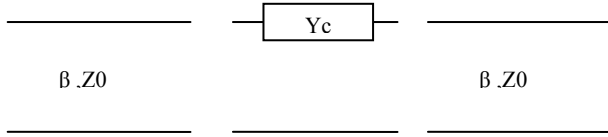


Fig. 5 Equivalent circuit of series capacitor on CPW

$$Y_C = Y_{Total} - Y_{Line}$$

$$Y_C = \frac{1}{R} + jwC$$

Y_c is in the form of $a + jb$ so

$$b = wC$$

$$C = \frac{b}{w}$$

V. SIMULATION

The software used for simulation of CPW line was MOMENTUM, is a lay out tool in Advance Design System software. It is an electromagnetic simulator. That computes the scattering parameter of planar structures and other topologies

A. Series capacitor

The design data of CPW line of characteristics impedance of 50 Ohm, and the series capacitor of 1.25pF are given in table The fig. 6 shows the momentum layout design .the design is simulated for a frequency range 1GHz to 10 GHz and the results are shown in figure 7

TABLE I. DESIGN VALUES OF SERIES CAPACITOR

CPW LINE	
Copper thickness	18um
Dielectric height	1600um
Dielectric constant	3.6
Strip width	3100um
Strip spacing	250um
Effective wave length	5200um
CAPACITOR	
2S	300um
2g	300um
l	200um
S1	150um

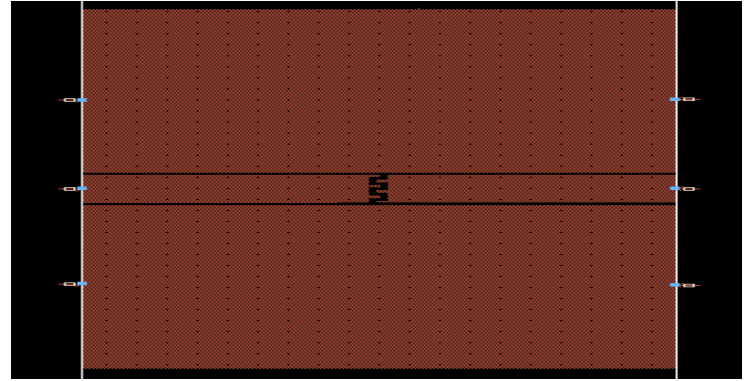


Fig. 6. Momentum layout

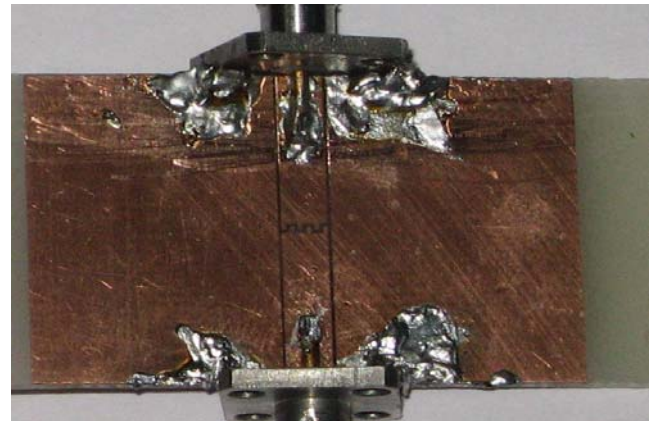


Fig. 7. Fabricated capacitor

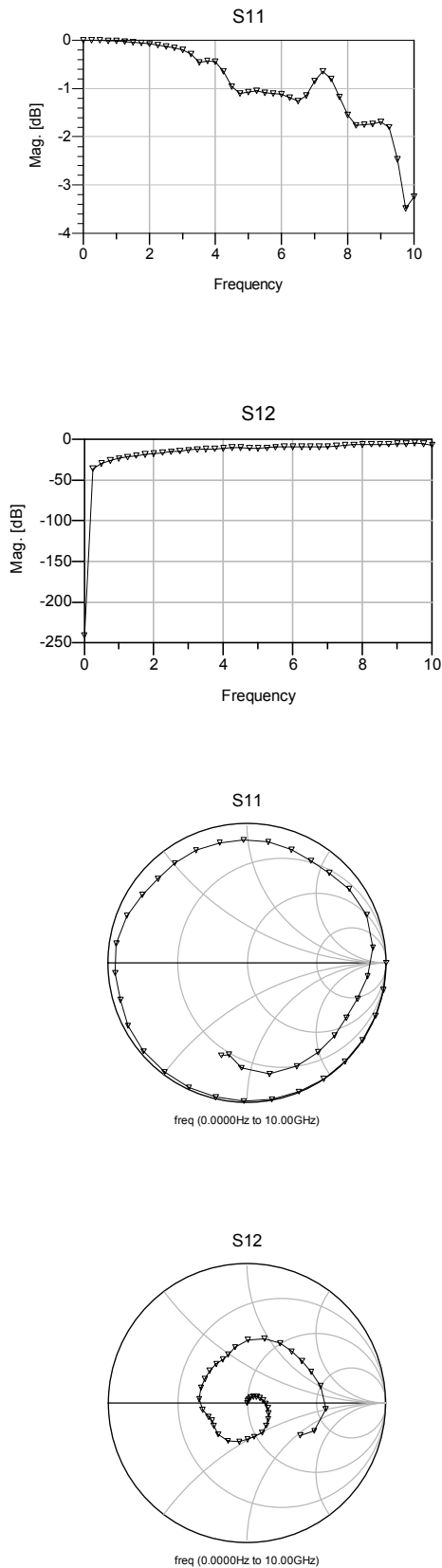


Fig. 7. Simulation results

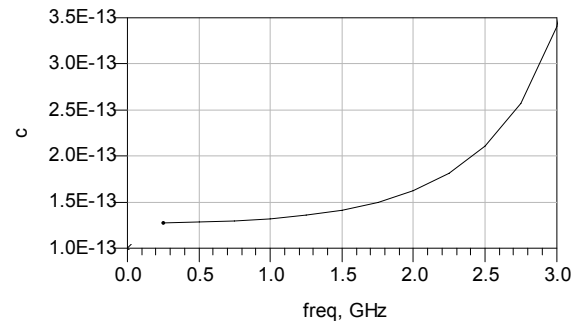


Fig. 8. Extracted Capacitance plot from simulation

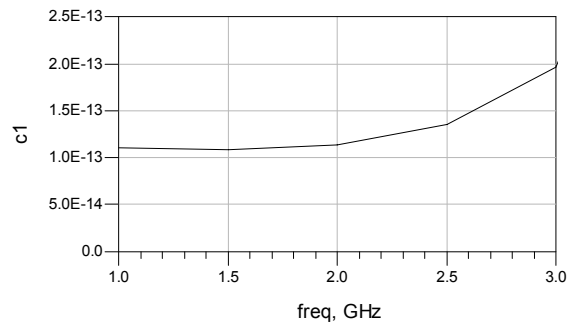


Fig. 8a. Extracted Capacitance plot from measurement

B. shunt capacitor

The design data of CPW line of characteristics impedance of 50 Ohm, and the series capacitor of 0.6pF are given in table

TABLE. II. DESIGN VALUES OF SHUNT CAPACITOR

CPW LINE	
Copper thickness	18um
Dielectric height	1600um
Dielectric constant	3.6
Strip width	3100um
Strip spacing	250um
Effective wave length	5200um
CAPACITOR	
2S	250um
2g	250um
L	250um
S1	5200um

The figure 9 shows the momentum layout design .The design is simulated for a frequency range 1GHz to 10 GHz and the results are shown in figure 11

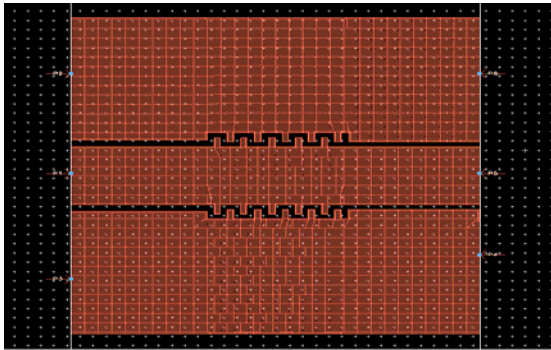


Fig. 9. Momentum layout

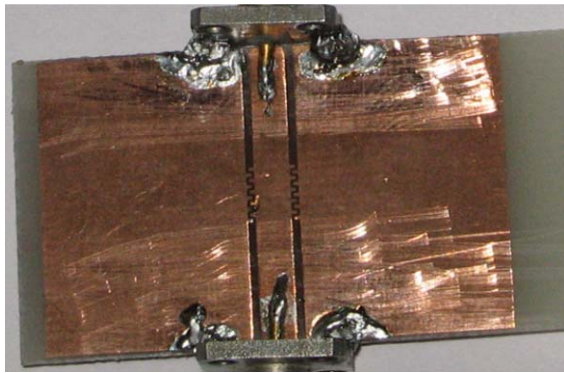


Fig. 10. Fabricated capacitor

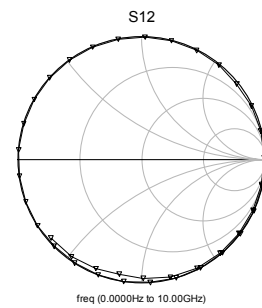
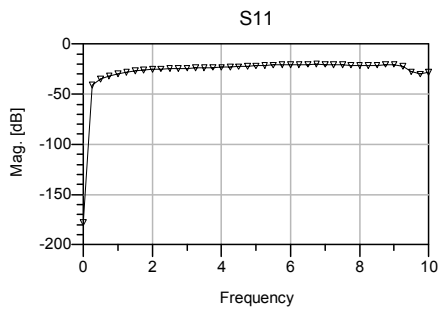
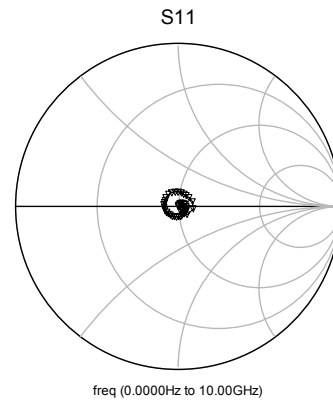
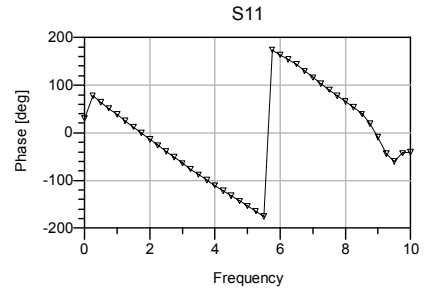
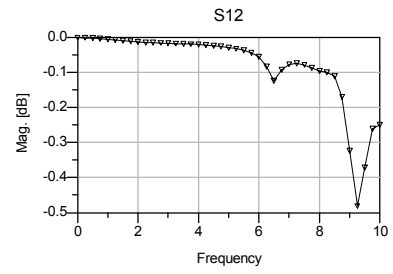


Fig. 11. Simulation results

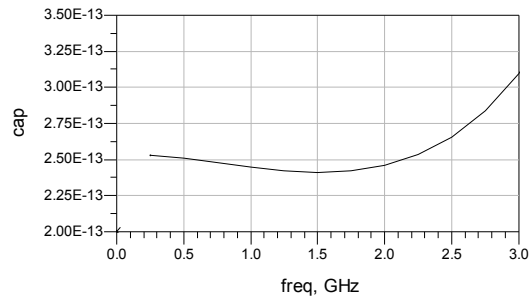


Fig. 12. Extracted Capacitance plot from simulation

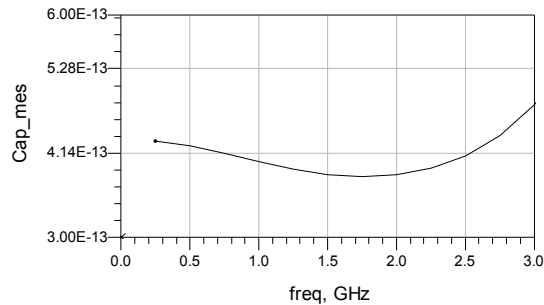


Fig. 12a. Extracted Capacitance plot from measurement

VI. MEASUREMENT

The capacitance structures are fabricated in printed circuit board (PCB), using PCB fabrication methods. The negative film of the structure is used to transfer the pattern to the PCB, the fabricated structure is measured using vector network analyzer (VNA). The S parameters measured using VNA are fed to the ADS Momentum using option add files, then the capacitance values are extracted using functions in ADS.

VII. CONCLUSION

The capacitor structures are simulated using software ADS Momentum, and realized on PCB. The capacitors constructed on PCB are measured using VNA. The simulation and measurement are not giving the capacitor values directly; the results are in terms of S parameters. Capacitances are calculated from the S parameters by converting into Z and Y parameters; the values are tabulated below.

TABLE I II. DE EMULATED CAPACITANCE VALUES.

capacitor	Design value	simulation	measured
Series capacitor	1.2E-13	2.1E-13	1.4E-13
Shunt capacitor	5.8E-13	2.6E-13	4.41E-13

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